Fermi National Accelerator Laboratory

FN-545

Programmable Digital Delay Unit

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Programmable Digital Delay Unit

At the request of E-774 we have designed and produced a six channel, single width Programmable Digital Delay Unit Camac module with 255 programmable delay steps of .5 ns each. The input and output levels are NIM and the connectors LEMO.

All the delays are programmed into the module using an 8 bit Camac word. All programmable registers can be read back as an eight bit word for checking and verifying data integrity. The programmable delays, PDU-18F-.5, are TTL devices manufactured by Data Delay Devices. They are available in other steps; .5 ns being the smallest available. There is an additional register that can be used to enable or disable any or all of the channels.

Minimum delays through each channel are less than 20 ns. The bulk of the delay being the programmable delay unit itself; 15 ns. The propagation delay could be reduced by a few nano seconds if the ECL version of this chip were used however it would be at the cost of many TTL to ECL translator chips on the board. This was deemed inappropriate for the intended use. There is no dead time associated with these units.

A complete schematic is available from the author.

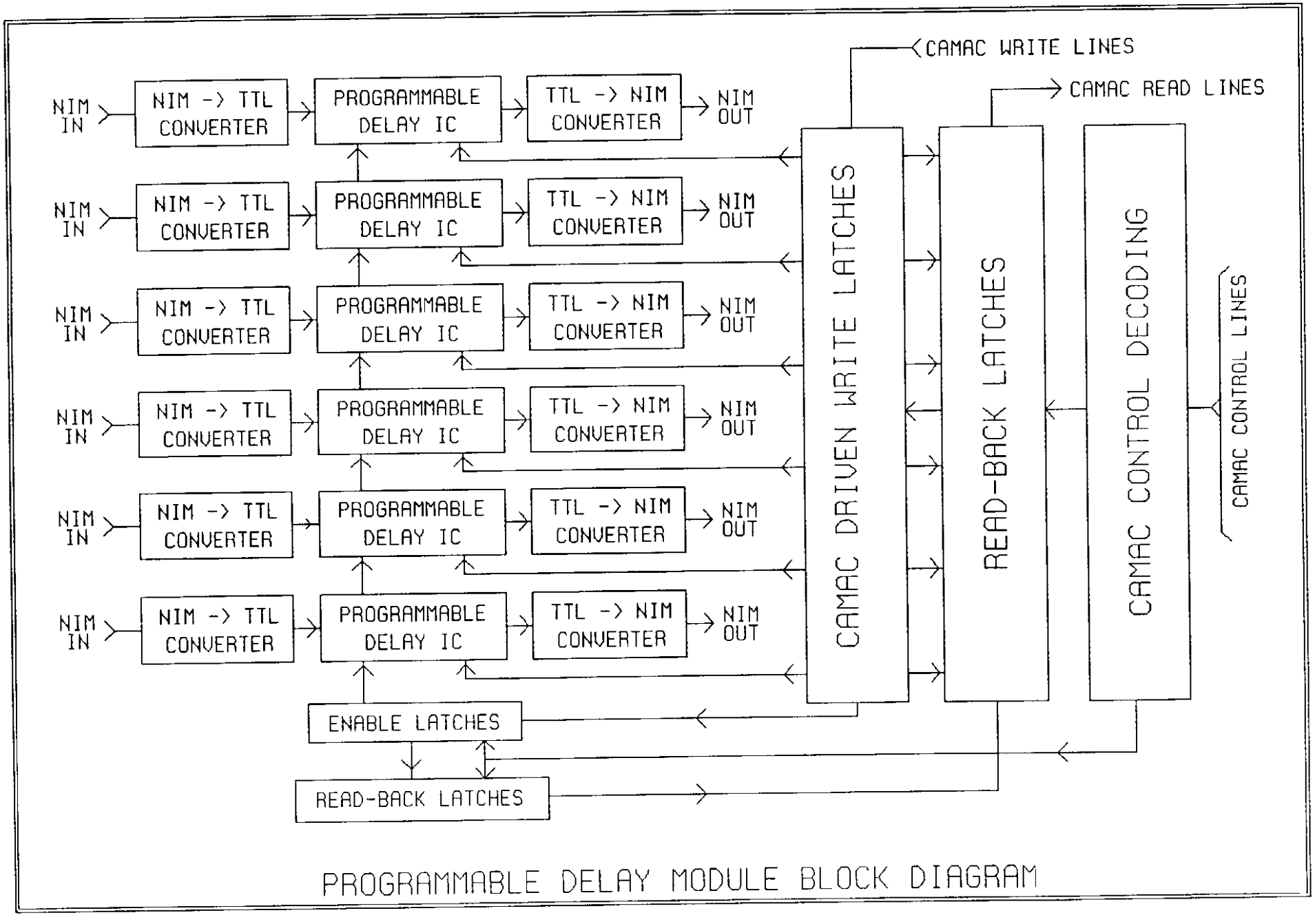
A block diagram is included.

Camac Commands:

N.F16.A1 -> A6	Writes 8 bit word to the delay latches.
N.F17.A0	Writes 6 bit word to the enable/disable register.
N.F9	Clears all registers, disables delay units.
N.F1.A1 -> A6	Reads 8 bit word from the delay latches.
N.F0.A0	Reads 6 bit word from the enable/disable register.

Each board costs about $500, the bulk of the expense being the delay units.

I wish to thank Mr. Robert Jones and Mr. Timothy May for their collective help in laying out the printed circuit board and constructive criticism.



PROGRAMMABLE DELAY MODULE BLOCK DIAGRAM